## CLAIMS

What is claimed is:

1. A logic circuit comprising:

a first look-up table (LUT) in a first logic element (LE), wherein the first LUT determines a carry; and

a second LUT in a second LE, wherein the second LUT determines a sum; and

an adder in the second LE, wherein the adder adds the carry and the sum.

2. The logic circuit of claim 1 further comprising:

a multiplexer in the second LE, wherein the multiplexer is coupled to the first LUT and a third LUT in the second LE, further wherein the multiplexer selects between a signal received from the first LUT and a signal received from the third LUT for forwarding to the adder.

3. The logic circuit of claim 1, wherein the adder comprises a hardwired adder.

4. The logic circuit of claim 1, wherein the first LUT determines a 1 bit carry of three binary numbers in a carry save adder process.

5. The logic circuit of claim 1, wherein the first LUT receives bits X[n], Y[n], and Z[n] and provides as an output ((X[n] AND Y[n]) OR (X[n] AND Z[n]) OR (Y[n] AND

Z[n])), wherein n is an integer, X[n], Y[n], and Z[n] are the n-th bits of binary numbers X, Y, and Z, further wherein OR designates the Boolean OR function, and AND designates the Boolean AND function.

6. The logic circuit of claim 1, wherein the second LUT determines a 1 bit sum of three binary numbers in a carry save adder process.

7. The logic circuit of claim 1, wherein the second LUT receives bits X[n+1], Y[n+1], and Z[n+1] and provides as an output (X[n+1] XOR Y[n+1]) XOR Z[n+1]), wherein n is an integer, X[n+1], Y[n+1], and Z[n+1] are the (n+1)-th bits of binary numbers X, Y, and Z, further wherein XOR designates the Boolean XOR (exclusive OR) function.

8. A programmable logic device including the logic circuit of claim 1.

9. A digital system comprising a programmable logic device including the logic circuit of claim 1.

10. A logic element (LE) comprising:

a multiplexer; and

an adder coupled to the multiplexer,

wherein the multiplexer selects between a signal determined in the LE and a signal determined in a previous LE for forwarding to the adder.

11. The LE of claim 10, wherein the adder comprises a hardwired adder.

12. The LE of claim 10 further comprising a first logic circuit that determines a sum of an (n+1)-th bit of three binary numbers in a carry save adder process, wherein n is an integer.

13. The LE of claim 12, wherein the logic circuit comprises a look-up table (LUT).

14. The LE of claim 10, wherein the previous LE comprises a second logic circuit that determines a carry of an n-th bit of three binary numbers in a carry save adder process, wherein n is an integer.

15. The LE of claim 14, wherein the logic circuit comprises a look-up table (LUT).

16. A programmable logic device including the LE of claim 10.

17. A digital system comprising a programmable logic device including the LE of claim 10.

18. A logic device comprising:

a first logic element (LE) including a first logic circuit, wherein the first logic circuit determines a carry in a carry save adder process; and

a second LE, wherein the second LE receives the carry.

19. The logic device of claim 18, wherein the second LE comprises:

a second logic circuit, wherein the second logic circuit determines a sum in the carry save adder process; and

a hardwired adder , wherein the first hardwired adder adds the carry and the sum.

20. The logic device of claim 19, wherein the first logic circuit comprises a first look-up table (LUT), further wherein the second logic circuit comprises a second LUT.

21. The logic device of claim 20, wherein the second LE further comprises:

a third LUT, wherein the third LUT determines a second carry in the carry save adder process;

a fourth LUT, wherein the fourth LUT determines a second sum in the carry save adder process; and

a second hardwired adder, wherein the second hardwired adder adds the second carry and the second sum.

22. The logic device of claim 21, wherein the second LE further comprises a fifth LUT, wherein the fifth LUT determines a third carry in the carry save adder process and provides the third carry to a third LE.

23. A programmable logic device including the logic device of claim 18.

24. A digital system comprising a programmable logic device including the logic device of claim 18.

25. A programmable logic device (PLD) comprising:

a first logic element (LE), the first LE including:

a first look-up table (LUT), wherein the first LUT determines a first sum;

a second LUT, wherein the second LUT determines a first carry;

a third LUT, wherein the third LUT determines a second sum;

a fourth LUT, wherein the fourth LUT determines a second carry;

a first hardwired adder, wherein the first hardwired adder receives the first sum from the first LUT and a carry from a LUT of a previous LE or ground signals; and

a second hardwired adder, wherein the second hardwired adder receives the first carry and the second sum; and

a second LE, the second LE including:

a fifth LUT, wherein the fifth LUT determines a third sum;

a sixth LUT, wherein the sixth LUT determines a third carry;

a seventh LUT, wherein the seventh LUT determines a fourth sum;

an eighth LUT, wherein the eighth LUT determines a fourth carry;

a third hardwired adder, wherein the third hardwired adder receives the third sum determined by the fifth LUT and the second carry determined by the fourth LUT; and

a fourth hardwired adder, wherein the fourth hardwired adder receives the fourth sum and the third carry.

26. The PLD of claim 25, wherein:

the first LE further comprises:

a first multiplexer having first and second input terminals and a first output terminal, wherein the first input terminal is coupled to one of ground signals or an output of the LUT of the previous LE, the second input terminal is coupled to a first output terminal of the second LUT, and the first output terminal is coupled to the first hardwired adder; and

a second multiplexer having third and fourth input terminals and a second output terminal, wherein the third input terminal is coupled to a second output terminal of the second LUT, the fourth input terminal is coupled to a first output terminal of the fourth LUT, and the second output terminal is coupled to the second hardwired adder; and

the second LE further comprises:

a third multiplexer having fifth and sixth input terminals and a third output terminal, wherein the fifth input terminal is coupled to a second output terminal of the fourth LUT, the sixth input terminal is coupled to a first output terminal of the sixth LUT, and the third output terminal is coupled to the third hardwired adder; and

a fourth multiplexer having seventh and eighth input terminals and a fourth output terminal, wherein the seventh input terminal is coupled to a second output terminal of the sixth LUT, the fourth input terminal is coupled to a first output terminal of the eighth LUT, and the fourth output terminal is coupled to the fourth hardwired adder.

27. The PLD of claim 25, wherein the first sum, the first carry, the second sum, the second carry, the third sum, the third carry, the fourth sum, and the fourth carry, are sums and carrys in a carry save adder process.

28. A digital system including the PLD of claim 25.

29. A method of adding binary numbers having multiple bits, the method comprising:

adding a carry determined by a first look-up table (LUT) of a first logic element (LE) with a sum determined by a second LUT of a second LE.

30. The method of claim 29 further comprising:

determining the carry; and

determining the sum.

31. The method of claim 30, wherein the determining the carry includes determining a 1 bit carry of three binary numbers in a carry save adder process.

32. The method of claim 31, wherein the determining the carry includes:

receiving bits X[n], Y[n], and Z[n]; and

determining ((X[n] AND Y[n]) OR (X[n] AND Z[n]) OR (Y[n] AND Z[n])), wherein n is an integer, X[n], Y[n], and Z[n] are the n-th bits of binary numbers X, Y, and Z, further wherein OR designates the Boolean OR function, and AND designates the Boolean AND function.

33. The method of claim 30, wherein the determining the sum includes determining a 1 bit sum of three binary numbers in a carry save adder process.

34. The method of claim 33, wherein the determining the sum includes:

receiving bits X[n+1], Y[n+1], and Z[n+1]; and

determining (X[n+1] XOR Y[n+1]) XOR Z[n+1]), wherein n is an integer, X[n+1], Y[n+1], and Z[n+1] are the (n+1)-th bits of binary numbers X, Y, and Z, further wherein XOR designates the Boolean XOR (exclusive OR) function.